Sem III CBGS (ETRX) 24/5/16.

Digital ckts & Design

QP Code : 30651

(3 Hours) **Total Marks: 80**

N.B.: (1) Question No. **1** is **compulsory**.

(2) Solve any **three** from remaining **five** questions.

(3) Draw neat **logic diagram** and assume **suitable data** wherever necessary.

Q 1 (a) Interfacing between CMOS and TTL 05

(b) Explain Shift Register and its applications 05

(c) PLA and PAL 05

(d) Draw truth table and logic diagram of Full Subtractor 10

Q 2 (a) Write a VHDL code for Full Adder 10

(b) Design MOD 8 asynchronous counter. 10

Q 3 (a) Design a mealy sequence detector to detect ---0101--- using D flip-flops and logic gates 10

(b) Design a circuit with optimum utilization of PLA to implement the following functions 10

$F1 = \sum m (0, 2, 5, 8, 9, 11)$

$F2 = \sum m (1, 3, 8, 10, 13, 15)$

$F3 = \sum m (0, 1, 5, 7, 9, 12, 14)$

Q 4 (a) Implement following function using 8:1 MUX and logic gates 10

$P (A,B,C,D) = \sum m (1,2,6,7,8,10,13,14)$

(b) Construct ring counter using IC 74194 and the output waveform 10

Q 5 (a) Use K-map to reduce following function and then implement it by NOR gates. 10

$F = \pi M (1, 2, 5, 8, 10, 12, 15) + d (0, 6)$

(b) Design 6 bit up counter using IC 74163, draw a circuit diagram and explain its working. 10

6. Write short notes on any **three** 20

i) JTAG and BIST

ii) Stuck at '0' and '1' faults

iii) XC 4000 FPGA architecture block diagram

iv) Noise Margins
